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Design of Highly Efficient CdSe Solar Cell with CdS as Buffer Layer Material

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Abstract- *As an absorber layer the performance of CdSe was numerically analysed in this research. Simulation was done by AMPS 1D simulator. CdSe material has a band gap of 1.74 eV which is near to the optimum band gap of photovoltaic solar cells. In the proposed cell, variation of layer thickness, doping concentration and temperature of the CdSe absorber layer was studied. CdS buffer layer was also optimized to get high efficient cell. The proposed structure shows highest performance than conventional cells. The efficiency of 15.36% was achieved by the proposed structure ITO/CdS/CdSe at 1.25 μm layer thickness of CdSe. The other output parameters are Jsc= 13.78 mA/cm^2, Voc= 1.30 V and FF= 0.870. If the thickness is increased up to 5 μm then the cell shows 18.66% efficiency. To reduce the cost 1.25 μm thickness is chosen.*

Keywords: CdSe Absorber Layer, CdS buffer Layer, Numerical Analysis, Output Parameters.

1. INTRODUCTION

The world is modernized and machines are taking places over humans. To operate the machinery work smoothly continuous power supply is required. The generation of electric power by using conventional energy are now questionable. These resources are not infinite in amount and consumption of these conventional energies cause damage to environment. So replacement of environment friendly energy resources are required. At this situation solar energy would be an effective solution. All the activities are centered by sun in this universe. For this among all the renewable energies, solar is the most abundant source of energy.

Majority of the group II-VI compounds, attracted interests of many researchers because of their contributions in optoelectronic devices [1]. Among II-VI compounds CdSe, CdS, CdTe etc. are leading because of their direct band gap properties and also for high absorption coefficients. No space charge region exist in nanocrystalline film and as a result charge separation is taken place by kinetic reaction. In various test it is proved that charge separation is effective with the presence of CdSe in a couple system. Properties of Zinc doped polycrystalline CdSe films was studied by Meera Ramrakhiani [2], where behavior of output parameters like *Voc*, *Jsc* corresponding to band gap is described. Optical and structural properties of thermally concentrated CdSe is studied by Cristian Baban [3] where absorption of CdSe is emphasized. D. pahinettam [4] with the help of CdSe powder purity of 99.99% observed that the band gap decreases while the layer thickness and substrate temperature increases. As nanocrystals semiconductors CdSe [5], PbSe [6-8], PbS [9-14] etc. are more effective for solar energy harnessing.

In the proposed work, p type CdSe layer of 1.25 μm was selected as an absorber layer. This selection was made from different observations from various thickness. Another n type CdS layer of 50 nm was selected as a window layer. P type material is striked by sun light over which Indium Tin Oxide (ITO) which is a transparent conducting oxide is connected as a front contact for increasing conductivity in this work. The rear surface is a metallic conductor which is connected as a back contact material. It provides an ohmic contact for the cell. Optimization of the structure with higher efficiency was done with the designed cell. 100 μm thickness of absorber layer is required for conventional silicon cell. In this proposed cell, absorber layer thickness is reduced 25 times than conventional silicon solar cell.

2. MODELING AND SIMULATION

The cell modelling and simulation of this work with ITO/CdS/CdSe structure were done by AMPS 1D. At 100 nm thickness of ITO with 50 nm thickness of CdS were used in the simulation work where the thickness range of CdSe material was 100 nm to 10000 nm. The high performance was chosen for 1250 nm layer thickness to reduce the cost. CdSe as an absorber layer has effective solar energy harvesting capability which reduces the cost of solar cells. The schematic arrangement of the proposed ITO/CdS/CdSe structure is shown in Figure 1.

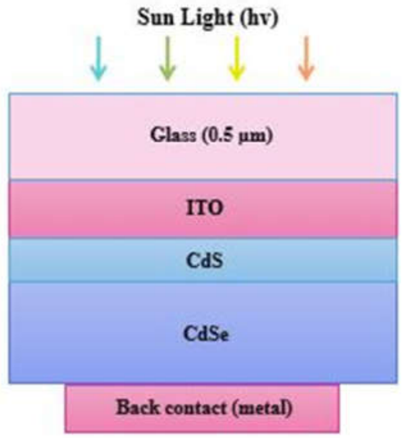

Fig. 1: The structure of CdSe solar cell

To observe the output performance parameters of proposed cell structure in the simulator, material parameters of ITO, CdS and CdSe must be needed. So the material parameters which is used in this work are shown in Table 1.

Table 1: Material parameters of CdSe solar cell

Parameters	i-ITO	n-CdS	p-CdSe
Thickness, W (nm)	100	50	100-5000
Permittivity, $\varepsilon/\varepsilon_0$	9	10	10.6
Band gap, Eg (eV)	3.6	2.40	1.74
Electron mobility, μc (cm^2/Vs)	100	100	650
Hole mobility, μp (cm^2/Vs)	25	25	50
Carrier concentration, n, p (cm^{-3})	1.7×10^{17}	1.0×10^{18}	1.0×10^{17}
Density of state in conduction band, Nc (cm^{-3})	2.2×10^{18}	2.2×10^{18}	2.75×10^{18}
Density of state in valence band, Nv (cm^{-3})	1.8×10^{19}	1.8×10^{19}	2.8×10^{19}
Electron affinity, χ (eV)	4.50	4.00	4.56

3. RESULT AND DISCUSSION

3.1 Effect of CdS Buffer Layer Thickness

Buffer layer thickness has a great impact on cell performance in ITO/CdS/CdSe solar cell. With the increase of thickness, performance parameter *Jsc* and Efficiency decrease. On the contrary, Fill Factor and Open Circuit Voltage shows a constant value and they have no impact on cell performance. At 50 nm thickness of CdS n type layer the performance parameters are: *Voc*= 1.28 V, *Jsc*= 13.66 mA/cm^2, *FF*= 0.876 and η= 15.36%. At 100 nm thickness the parameters are: *Voc*= 1.28 V, *Jsc*= 13.39 mA/cm^2, *FF*= 0.876 and η= 15.06%. And finally *Voc*= 1.28 V, *Jsc*= 12.41 mA/cm^2, *FF*= 0.876 and η= 13.93% for 500 nm thickness of CdS. 50 nm thickness was chosen for better operation of the cell.

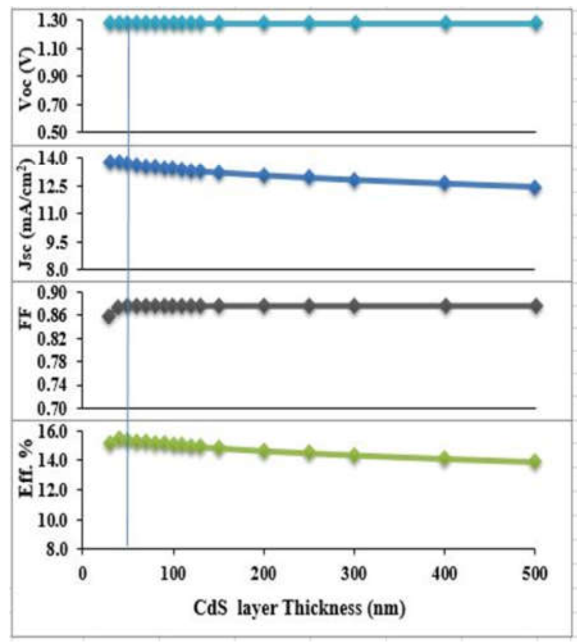

Fig. 2: Effect of CdS buffer layer thickness on cell performance

3.2 Effect of CdSe Layer Thickness

Variation of absorber layer thickness changes the output parameters of solar cell. With the increase of CdSe layer thickness, the output parameters *Voc, FF* and *η* (efficiency) increase. On the contrary open circuit voltage, *Voc* shows a constant value. In this work, 1.25 μm layer thickness is chosen for CdSe which shows the high output parameters. After that thickness the performance also increase but cost will be higher for high layer thickness. So implementation will be difficult. The output cell performance parameters at 1.25 μm thickness are: *Voc*= 1.28 V, *Jsc*= 13.66 mA/cm^2, *FF*= 0.876 and η= 15.36%. Efficiency is mainly affected by *Voc* and *Jsc* during the layer thickness variation. The cell performance for variation of layer thickness of CdSe absorber layer from 0.1 μm to 5.0 μm is given below.

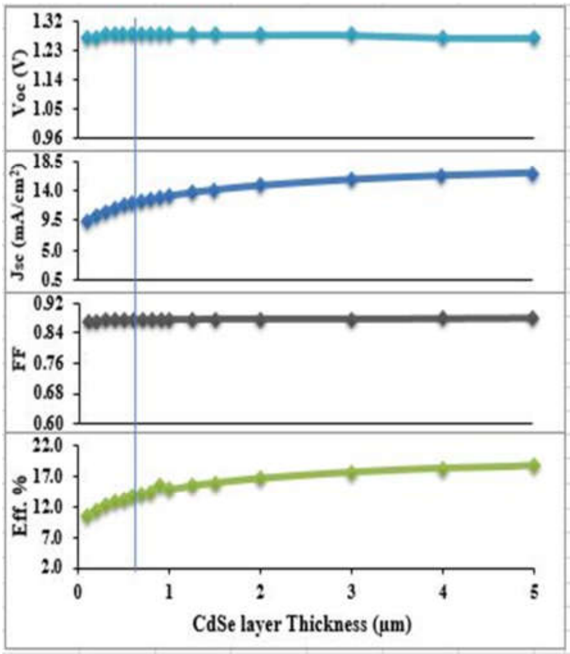

Fig. 3: Effect of CdSe absorber layer thickness for the proposed solar cell structure.

3.3 Effect of Doping Concentration

Doping concentration of CdSe absorber layer is varied from 1.0×10^{13} to 1.0×10^{18} cm^{-3}. It can be observed that *Voc, Jsc*, *FF* and Efficiency increase with the increase of doping concentration. From the total observation it is observed that after 1.0×10^{17} cm^{-3} doping the cell performance decrease. The parameters *Jsc, FF* and Efficiency decrease and *Voc* increase.

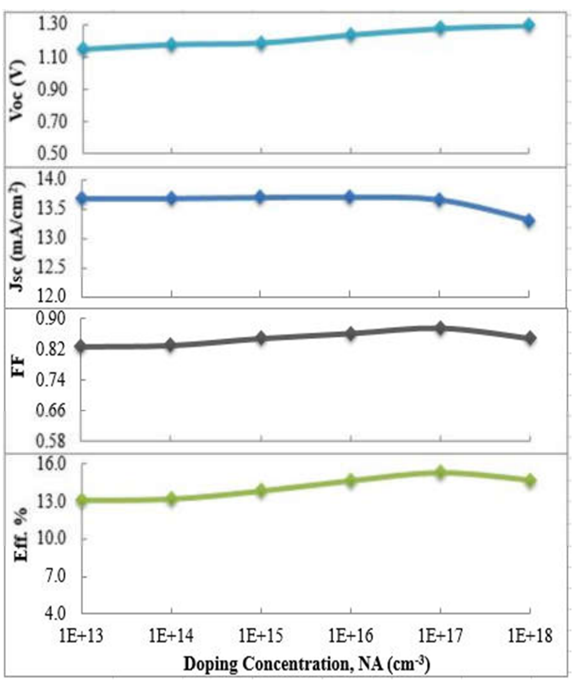

Fig. 4: Effect of CdSe doping on cell performance

1.0×10^{17} cm^{-3} doping is chosen for the perfect operation. At 1.0×10^{15} cm^{-3} doping the output parameters are: *Voc*= 1.19 V, *Jsc*= 13.69 mA/cm^2, *FF*= 0.849 and η= 13.86%. At 1.0×10^{17} cm^{-3} doping concentration the output parameters are: *Voc*= 1.28 V, *Jsc*= 13.66 mA/cm^2, *FF*= 0.876 and η= 15.36% and finally at 1.0×10^{18} cm^{-3} doping the output parameters are: *Voc*= 1.30 V, *Jsc*= 13.32 mA/cm^2, *FF*= 0.849 and η= 14.75%.

3.4 Effect of Temperature

Cell performance mostly depends on operating temperature. Temperature variation is needed to test the thermal stability of solar cells. In this research work performance of this cell is examined for higher temperature. High operating temperature affects the electron-hole mobility, carrier concentration, density of states and band gap of the materials. Our research simulations were operated at temperature ranging from 25°C to 105°C. Cell performances decrease with the increase of operating temperature. Open circuit voltage (*Voc*) and Fill Factor (*FF*) decrease but short circuit current density (*Jsc*) remain constant. So overall cell efficiency decreases with the increases of operating temperature. Cell performance results at various temperature are shown in Figure 5.

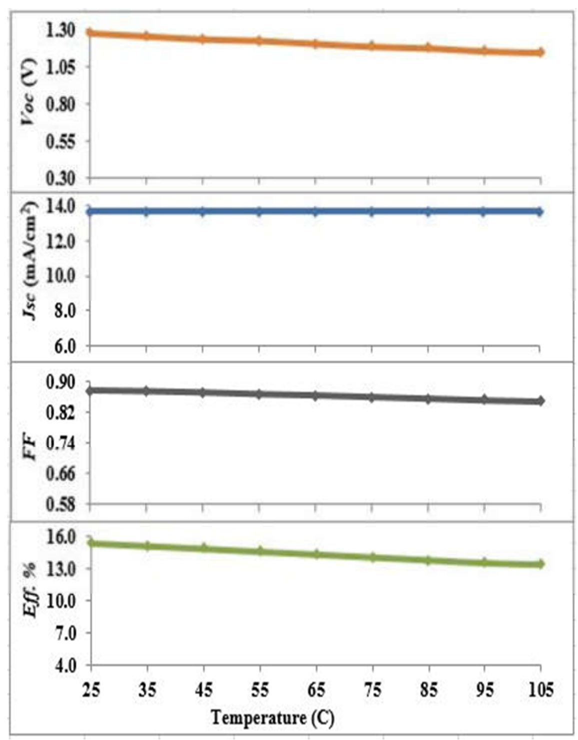

Fig. 5: Effect of the operating temperature on cell performances.

The Fig. 6 shows normalized efficiency Vs operating temperature. The cell efficiency linearly decreased with the increase of temperature. Normalized value of efficiency 1 is selected for 25°C operating temperature.

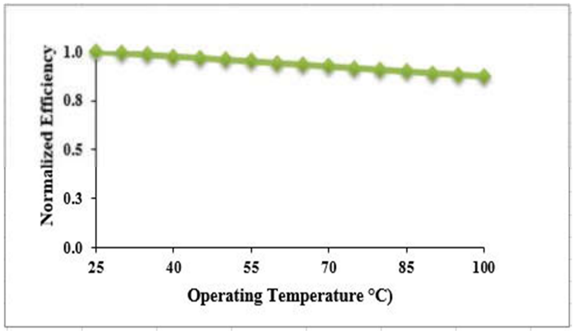

Fig. 6: Effect of operating temperature on normalized efficiency.

3.5 Effect of TCO Layer

Indium Tin Oxide (i – ITO) was used in this cell as TCO layer for transparency and conductivity of solar light. Output performances increase if the TCO is inserted in cells. Over 3 eV band gap of TCO layer can cover the visible wavelength range of light radiation and the resistivity of layer should be as low as possible. Table II shows the performance of CdSe solar cell with and without TCO layer.

Table 2: Comparison of Output Performance with and without TCO Layer

Parameters	Voc (V)	J_{SC} (mA/cm^2)	FF	Eff. (%)
With TCO	1.28	13.66	0.876	15.36
Without TCO	1.27	12.06	0.875	13.49

4. J-V CHARACTERISTICS CURVE OF CdSe SOLAR CELL

Short circuit current (*Jsc*) will be maximum when open circuit voltage (*Voc*) is zero. The maximum short circuit current is 13.66 mA/cm^2. Again *Voc* will be maximum at zero *Jsc*. The maximum *Voc* of our cell is 1.28 V. The *J-V* curve is shown in Fig. 7.

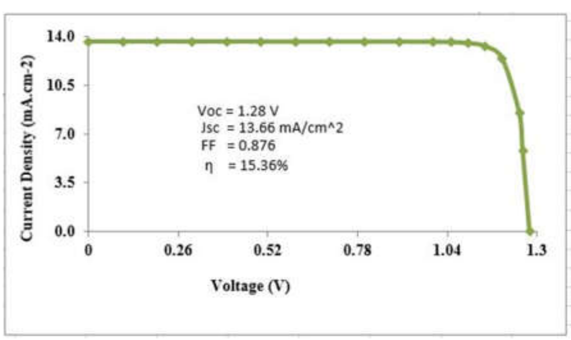

Fig. 7: J-V characteristics curve of proposed CdSe solar cell.

5. CONCLUSION

CdS buffer layer (50 nm) with transparent ITO layer (100 nm), the high cell performances were chosen for 1.25 μm layer thickness of CdSe material. The highest conversion efficiency is obtained 15.36% with *Jsc* =13.66 mA/cm^2, *FF* =0.876, *Voc* =1.28V. If the cell thickness is increased to 5 μm then the conversion efficiency = 18.66% with *Jsc* =16.60 mA/cm^2, *FF* =0.880, *Voc* =1.22V. On the contrary, 12% efficient Photoelectrochemical (PEC) solar cell using CdSe was introduced by B. Heller Miller et al [15] and Photoelectrochemical (PEC) CdSe solar cell introduced 9.2% efficiency by A.B. Ellis et al [16].

6. ACKOWLEDGEMENT

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